LOW SWITCHING POWER LIMITED SWITCH DYNAMIC LOGIC

ABSTRACT OF THE DISCLOSURE

An LSDL circuit is improved by having the data input function to control the pre-charging of the dynamic node. The clock signal no longer is coupled to the P channel FET used to pre-charge the dynamic node. Additionally an N channel FET (NFET) is added in parallel with the NFET coupled to the clock for evaluating the dynamic node. This NFET assures the dynamic node does not float when the data input is a logic one and the clock is a logic zero.

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